REMARKS/ARGUMENTS

Claims 1-23 were pending in this application. Upon entry of this amendment, claims 1, 2, 8, 9, 13, 15, and 16 are amended, new claims 24 through 27 are added, leaving claims 1-27 pending consideration. Claims 1, 3-8, 18, 20, and 23 stand rejected under 35 U.S.C §103(a) over U.S. Patent Application Publication No. 2020159483 published to Clauberg (hereinafter "Clauberg") in view of U.S. Patent No. 5,652,878 issued to Craft (hereinafter "Craft"). Claims 2, 9, and 13 stand rejected under 35 U.S.C §103(a) over Clauberg and Craft, in further view of U.S. Patent No. 6,747,886 issued to Morikawa (hereinafter "Morikawa"). Claim 21 stands rejected under 35 U.S.C §103(a) over Clauberg and Craft, in further view of U.S. Patent No. 6,160,419 issued to Veenstra (hereinafter "Veenstra"). Claims 10-12, 14-17, 19 and 22 are objected to. Applicants aver that no new matter has been added in this response.

Objections

In the Office Action, the Examiner objected to claims 2, 9, 10-13, and 15-16 for various informalities. Applicants have amended claims 2, 9, 10-13, and 15-16 to more clearly recite the claimed subject matter, and believe that the objections are now moot.

§103 Rejections

Claims 1 and 8

In the Office Action, the Examiner rejected claims 1, 3-8, 18, 20, and 23 under 35 U.S.C §103(a) over Clauberg in view of Craft, and claims 2, 9, and 13 in further view of Morikawa, and claim 21 over Clauberg in view of Craft and in further view of Veenstra.

With regard to claims 1 and 8, the Examiner states that Clauberg in combination with Craft teaches a method of receiving a serial stream of data bits, deserializing the stream of data bits, inputting the parallel bits into a register via a de-multiplexer, inputting an output of the first register to a second register, and providing the parallel bits in a plurality of parallel bit output formats, where the shift register is capable of shifting the outputted data into any of the plurality of parallel formats, citing paragraph 23, and paragraph 32, and Figure 2, *et seq.* of

Clauberg, columns 2 and 3 *et seq.* of Craft, Figure 3 and column 3 *et seq.* of Morikawa, and Column 1 and 2, *et seq.* of Veenstra. These rejections are respectfully traversed.

For at least the reasons stated below, the Applicants respectfully request reconsideration and withdrawal of the rejections, as each of the claims as amended are patentable over the cited art, alone or in combination.

For example, claim 1 as amended recites in part "providing a bus configured to receive .. parallel bits and output of [a] first register, wherein the data lines forming the bus are grouped into a plurality of overlapping subsets of the bus that each contain at least one common data line," and "selecting one of the parallel bit output subsets of the bus based on match flag outputs from [a] content addressable memory, wherein the match flag outputs are generated in response to the inputs to the content addressable memory". Claim 8 as amended recites in part, "a deserializer circuit coupled to receive serial data input and outputting a first parallel data output, wherein the deserializer circuit outputs the first parallel data onto a bus that is configured with overlapping subsets of the bus, wherein the subsets include at least one common data line". The Applicants submit that Clauberg, Craft, Morikawa, or Veenstra, alone or in combination, fail to disclose at least these elements of claim 1 or 8.

The frame byte alignment system and technique disclosed in Clauberg is directed to a fundamentally different system and technique than the claimed subject matter. For example, Clauberg discloses deserializing an incoming serial data stream into a 16 bit parallel data stream using a deserializer. The 16 bit parallel data output stream is converted to an unaligned 64 bit word stored in a first register 214. Over three clock cycles, three 64 bit words are stored in a second register to form a 192 bit word. An align position detection unit 218 locates the specific bit pattern indicating the beginning of a new frame (e.g., A1A2) by "hunting" along the 192 bit word to find the correct 64 bit section. An extraction unit 222, extracts the 64 bit section of the 192 bit word and sends that to an output port 204. Craft discloses using a CAM to store data; Morikawa discloses a level sifting circuit; and Veenstra discloses a CAM to store keywords associated with datawords stored in another functional block. In Veenstra, if a request dataword matches one of the keywords, the second functional block outputs the dataword stored therein associated with the matching keyword.

Neither Clauberg , Craft, Morikawa, nor Veenstra, alone or in combination, disclose *deserializing the incoming serial data to form parallel bits that are input into a register, outputting the parallel bits and output from the register on a bus, and then grouping the data on the bus into a plurality of parallel bit output subsets that share at least one data line* (emphasis added). For example, Clauberg discloses the output of the third register as a three distinct groupings of parallel data (e.g., 63:0, 127:64, and 191:128) from each of the three clock cycles, where the output of each of the groupings do not share at least one common data line. Claims 1 and 18 are thus patentably distinguished over Clauberg , Craft, Morikawa, or Veenstra for at least the above reasons.

Dependent Claims 2-7, and 9-23

Claims 2-7 depend from amended claim 1, and claims 9-23 depend from amended claim 8, and are therefore patentable for at least the above reasons. These claims, however recite additional elements that further distinguish over the cited art. For example, with regard to claims 2-7, claim 2 partially recites the "parallel bits and the output of the first register are input to a plurality of tristate driver circuits", claim 3 partially recites, eight parallel bits, claim 4 partially recites, "wherein the first and second registers are two stages of a shift register", claim 5 partially recites "wherein a depth of the content addressable memory comprises at least one row for each of the parallel bits", claims 6 and 7 partially recite "wherein the inputs to the content addressable memory are provided by way of parallel transfer". With regard to claims 13, 18, 20-21, and 23, claim 13 partially recites "wherein there is one parallel data output for each bit of the first parallel data output minus 1", claim 18 partially recites "wherein the content addressable memory has a number of rows equal to or greater than a number of bits of the first parallel data output", claim 20 partially recites "wherein the first parallel data output is 8, 10, 16, or 20 bits wide", claim 21 partially recites a "programmable logic integrated circuit", and claim 23 "wherein the first parallel data output comprises 8 bits in a format bit 0, bit 1, bit 2, bit 3, bit 4, bit 5, bit 6, and bit 7". The cited art does not disclose at least the elements, alone or in combination.

Allowable Subject Matter

In the Office Action, the Examiner Stated that claims 10-12, 14-17, 19, and 22 are objected to but would be allowable if written in independent form.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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